



## STUDY AND CONSTRUCTION OF A SUCCESSIVE APPROXIMATION ADC8K FOR MULTICHANNEL ANALYZER SYSTEM

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### ABSTRACT

Multi-channel Analyzer (MCA) is one of very essential equipment in nuclear physics and nuclear engineering for the measurement of ionization radiation. Generally, an MCA system consists of radiation detector, amplifier system, ADC circuit, and MCD connected with computer for data processing. Among them, ADC is a functional electronic block, which plays an important role for converting analog to digital signals. Corresponding to the domestic needs in development of nuclear instruments, this work presents a design and construction of an ADC8K module with successive approximation method. Some experimental results are as follows: Differential non-linearity (DNL%) = 1.42, Integral non-linearity (INL% = 0.58), and  $\chi^2 = 8.109$  proved that mentioned system can be used with considerable reliability in practical nuclear engineering.

**Keywords:** DNL, INL,  $\chi^2$ , Successive approximation.

### TÓM TẮT

**Nghiên cứu và xây dựng khối ADC8K xấp xỉ liên tiếp dùng trong hệ máy phân tích đa kênh**

Hệ máy phân tích đa kênh (MCA) dùng trong ghi đo bức xạ ion hóa là một trong những hệ thống thiết bị rất cần thiết trong nghiên cứu vật lý và kỹ thuật hạt nhân. Một hệ MCA hiện nay thường bao gồm đầu dò, bộ khuếch đại, mạch ADC, mạch MCD ghép nối máy tính để xử lý kết quả đo; trong đó, mạch ADC đóng vai trò quan trọng trong việc chuyển đổi tín hiệu tương tự thành tín hiệu số. Bài báo này trình bày việc nghiên cứu xây dựng khối ADC8K theo phương pháp biến đổi xấp xỉ liên tiếp. Các tham số đặc trưng kỹ thuật đạt được bao gồm: độ phi tuyến vi phân (DNL% = 1.42), độ phi tuyến tích phân (INL% = 0.58),  $\chi^2 = 8.109$  minh chứng hệ thống có thể ứng dụng khả thi trong các nghiên cứu thực nghiệm trong lĩnh vực kỹ thuật hạt nhân.

**Từ khóa:** DNL, INL,  $\chi^2$ , xấp xỉ liên tiếp.

### 1. Introduction

Da Lat University is in charge of specialized training in nuclear engineering, but the equipment used in research and experimental measurement is not fully equipped and needs to be supplemented. Therefore, the construction of multi-channel analysis systems, gamma-ray measurement and experiments to improve the level of research for students and graduate students in the field of engineering physics is one of the urgent needs. At present,

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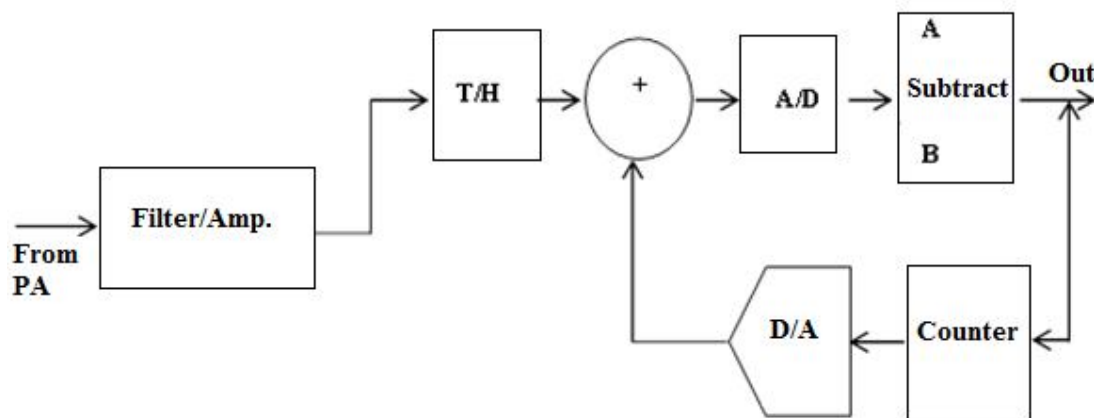
the orientations of research in the field of Engineering Physics are aimed at improving knowledge and skills in design and fabricate of nuclear equipment, gamma radiation measurement and exploitation and operation of experimental equipment. The design and fabricate of gamma spectrometer using high-quality radiation detector will support the method of constructing nuclear electronics instruments, collecting and processing spectra of experiments. In fact, the analog to digital converter is a very important key in this system. The objective of the project is to study and construct the ADC8K block to form a nuclear instrumentation system for gamma measurement used in nuclear engineering training. The work is presented in two theoretical and experimental parts, in which the characteristics and primacy of the ADC and the implementation of the channel width uncertainty compensation (Sliding scale method) is mentioned. In order to implement the aforementioned content, the application methods are:

- Channel width modulation method to correct the uncertainty of width between channels within the range of the ADC for enhancement of the resolution of the total energy peak in the energy spectrum.
- Successive approximation (SAR) method to improve the linearity between the recorded count and the input signal amplitude.

## 2. Design and methods

### 2.1. The working principle of the channel width correction circuit

The role of channel width correction circuit using sliding scale method is to adjust the channel-to-channel uniformity and to linearize the input energy amplitude. Thus, the energy resolution of the corresponding spectral peak is improved and this method is very effective [1] when applied to the practical ADC design used in nuclear physics experiments. The channel width correction is shown in Figure 1.



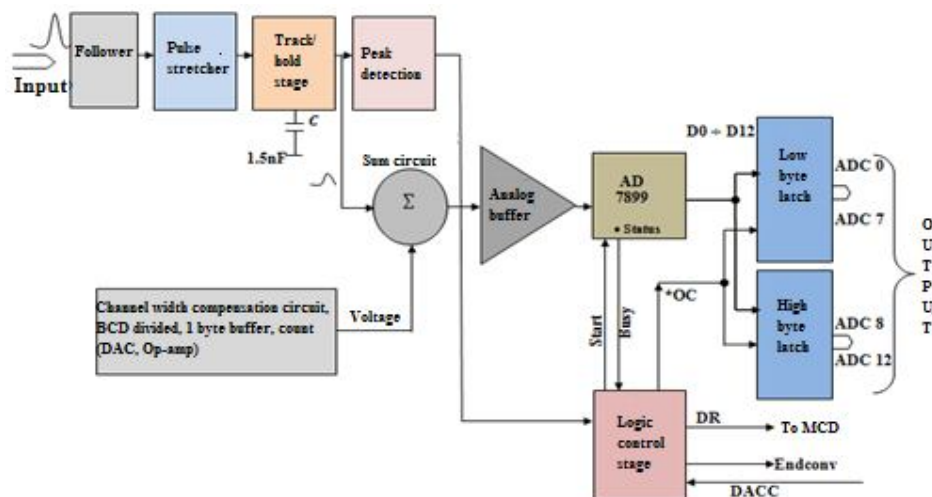
*Figure 1. Channel width correction stage*

The analog signal from the track/ hold (T / H) output will follow the statistical distribution as the peak is scattered by the odd-even effect. The result is a poor energy resolution and this phenomenon is overcome by the mixing of the signal T / H and the output of the digital to analog converter (D / A). The D / A consists of a digital-to-analog converter (DAC 0800) and an LF356 Op-amp. Once mixed, the output of the mixing layer is transformed by the A / D converter (chip used is AD7899) converted into 13-bit binary digits in 2.2 $\mu$ s. This digit is subtracted from the 8-bit binary digit (formed by the 8-4-2-1 counter using 74LS393: 1/2 byte); At the same time, this digit is sent to the D / A to form an analog signal mixed at the adder. Thus, results 13bit binary digit output has been overcome the heterogeneity of the channel width.

## 2.2. Design, fabricating 8K SAR ADC

### 2.2.1. Block structure diagram

The block diagram of the SAR 8K ADC is shown in Figure 2.



**Figure 2.** Block diagram of the 8K ADC

### 2.2.2. Operational principles and timing requirement

Unipolar positive output signal with sufficient amplitude from the spectroscopy amplifier is sent to the ADC input. This signal circuit keeps the same status by repeated input. Pulse stretcher of the peak expands the charge-discharge time corresponding to the rising and falling edges of the signal. This operation is done by the hold and sampling circuit through the C storage capacitor. The stored signal on the C-capacitor is split into two branches. It performs two tasks: the logic pulse shaping to the logic control, which informs the ADC7899 that the peak detection circuit has detected the peak state [2]; at the same time, the analog signal is sent to the adding circuit. The adding circuit mixes the

above-mentioned signal and the corrected signal about the channel width error. As a consequence, the output signal of the adding circuit is required for the homogeneous properties of the channels and this signal is applied to the input of the AD7899 converter after the pulse correction has been made. Let the AD7899 converter operate, the circuit needs a logic control. The logic controller is on duty as follows: start signal is sent to notify this IC AD7899 knew that conversion cycle begins, then analog input signal is converted from analog to digital. During operation, the AD7899 performs a  $2.2 \mu\text{s}$  conversion cycle that satisfies 13 bits. At the end of a cycle, the AD7899 converter outputs a status signal which tells the logical control stage that the digital BCD data is ready for validation on the internal output bus. The length of time from the beginning of conversion to the end of a 13-bit cycle is the busy time of AD 7899; this time is expressed by the interval of Busy signal. In addition to the Busy conversion of the AD7899, the ADC converter also has an internal deadtime of the conversion process; therefore the ADC deattime is equal to Busy plus internal deadtime. As a result, the total deadtime (DT) is sent to the MCD interface to process. The 13-bit internal data at the output of AD7899 is temporarily written into the two low (D0 ÷ D7) and high (D8 ÷ D12) data bytes. Thanks to the low valid OC signal, the data in the two latch bytes will be active at the 13-bit ADC address output from ADC0 to ADC12. After completing conversion, the ADC sends the DR signal to the MCD that the data has been validated and ready to be sent to it. Assuming that the connection between the ADC and the MCD is correct, the MCD side immediately receives the DR signal to process the data sent by the ADC side. After the processing is complete, the MCD signal DACC notify ADC knowing that such data set has been accepted; The second conversion cycle was initiated [4]. This process is repeated until the required time of acquisition and processing of the data terminates. The conversion cycle of the ADC is shown in timing requirement in Figure 3.

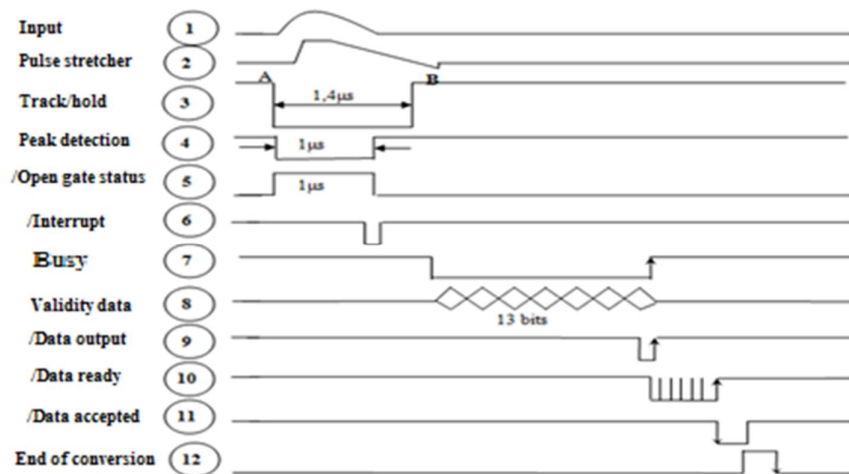


Figure 3. Timing requirement of 8K ADC

## 2.2.3. Flowchart and its explaining algorithm

The ADC8K flowchart is shown in Figure 4. In its initial state, the ADC is initiated. The output signal from the spectroscopy amplifier (1) is polynomially tested, and if the Gaussian, single, positive polarization is satisfied, the signal is repeated by the input follower. As shown in timing requirement, the output of the follower will be converted to a time-varying signal from the beginning of  $t_A$  and the end time  $t_B$  by the pulse stretcher (2). The pulse peak stretching signal is loaded into store capacitor and through the track/hold circuit (3), the peak of pulse (4) is detected. This peak is the first digital signal that allows the A / D converter to recognize the start of a conversion from analog to digital. The condition for the peak to be detected is that the track/ hold signal must satisfy the threshold condition and the energy window. Assuming that the peak is detected, the input of the flip-flop will be opened (5, 6) to allow the conversion beginning. The conversion cycle is performed by the AD7899 in parallel with the 13-bit conversion time of  $2.2 \mu s$ . If this condition is met, the binary digit will be validated on the internal bus (8) at the output of AD7899. This data will be latched in 2 bytes (low and high) through the latch enable signal (9). For the MCD side knowing that the ADC conversion has been completed, the ADC generates a ready signal (10) to send data to the MCD. If the data condition is not satisfied, the ADC continues to export the data internally, whereas this data will be read when the MCD accepts it. After completing the ADC data acceptance task, the MCD will send the processed message (11) to the ADC. As a result, the radiation spectrum is displayed by the application software and termination process.

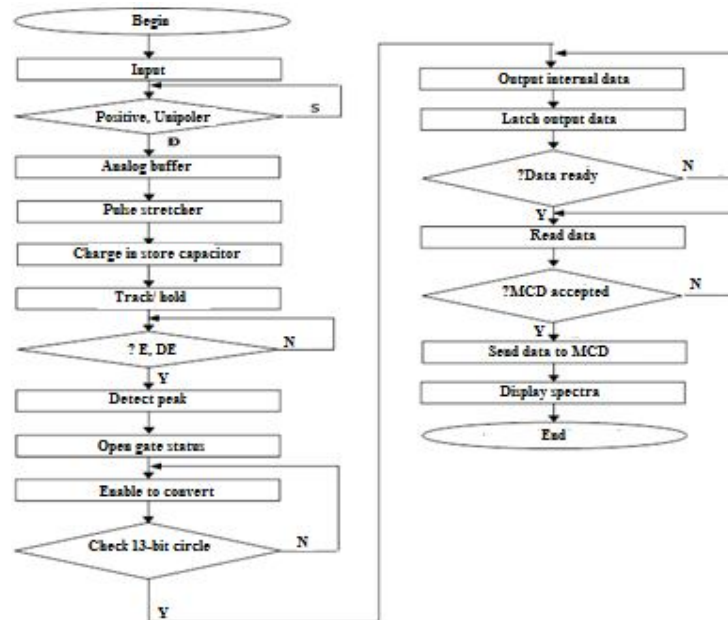


Figure 4. Flowchart of ADC8K

### 3. Experiments and comments

#### 3.1. Integral Nonlinearity (INL) Test

To test the INL of the ADC8K, the experimental configuration is shown in Figure 5. The acquisition and processing program used is MCANRI.exe (developed by VC++) to control the MCD8K-multichannel data processing unit.

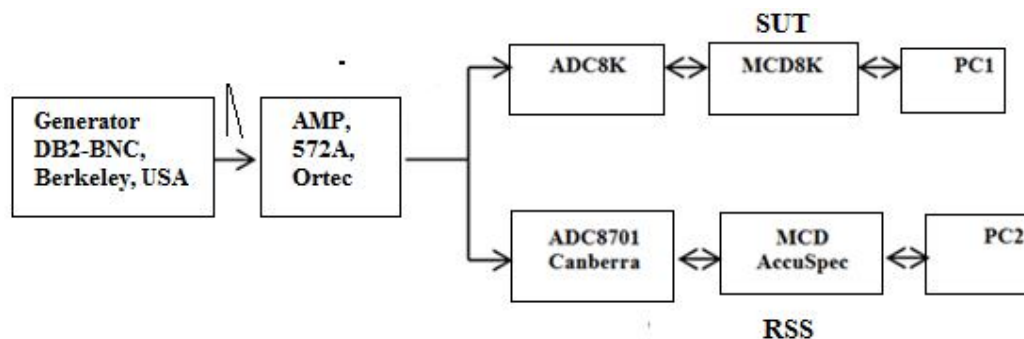


Figure 5. Configuration for Integral Nonlinearity test

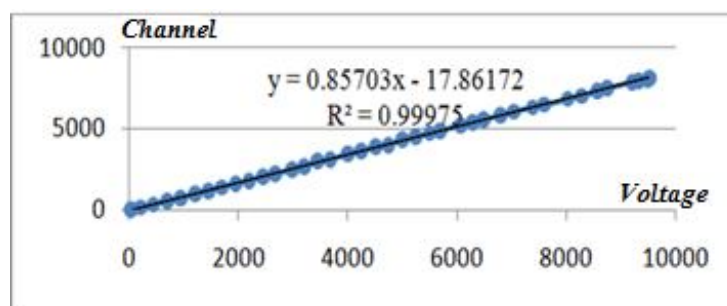
The DB2-BNC type pulse generator, Berkeley, USA generates a positive, single pole signal, 50 ns rising time, and 20  $\mu$ s falling time, lower threshold LLD  $\approx$  22 mV, upper limit ULD  $\approx$  10000 mV. In principle, the input signal amplitude proportional to the energy and amplitude will scan the 8192 entire channel range. To achieve that, adjustment step by step incrementally from 0 to 10.000 mV, the number of steps to check is 40. The corresponding value pairs of voltages and channels are listed in Table 1.

Table 1. Value of voltage-channel pairs obtained during  $INL_{ADC8k}$  test

STT	Thế (mV)	$C_r$	$C_i$	$\Delta C$	STT	Thế (mV)	$C_r$	$C_i$	$\Delta C$
1	21	26	4.839	-21.161	21	4984	4321	4249.793	-71.207
2	195	164	153.665	-10.335	22	5241	4491	4469.610	-21.390
3	435	335	358.942	23.942	23	5491	4733	4683.440	-49.560
4	694	574	580.470	6.470	24	5683	4891	4847.661	-43.339
5	937	751	788.313	37.313	25	6054	5218	5164.985	-53.015
6	1195	977	1008.985	31.985	26	6272	5381	5351.445	-29.555
7	1447	1205	1224.526	19.526	27	6472	5545	5522.509	-22.491
8	1693	1401	1434.935	33.935	28	6783	5828	5788.513	-39.487
9	1942	1603	1647.909	44.909	29	7038	6059	6006.620	-52.380
10	2187	1823	1857.463	34.463	30	7375	6307	6294.863	-12.137
11	2447	2037	2079.846	42.846	31	7579	6483	6469.348	-13.652

12	2658	2231	2260.318	29.318	32	8016	6826	6843.123	17.123
13	2972	2494	2528.889	34.889	33	8275	7019	7064.651	45.651
14	3203	2687	2726.468	39.468	34	8555	7306	7304.140	-1.860
15	3436	3032	2925.757	-106.243	35	8733	7508	7456.387	-51.613
16	3673	3104	3128.468	24.468	36	9195	7814	7851.545	37.545
17	3987	3479	3397.039	-81.961	37	9317	7931	7955.894	24.894
18	4238	3648	3611.724	-36.276	38	9482	8050	8097.022	47.022
19	4507	3893	3841.805	-51.195	39	9517	8115	8126.958	11.958
20	4738	4011	4039.384	28.384	40	9519	8121	8128.669	7.669

From the table of recorded data, the first order fit and the equation of the fit line is  $y = 0.85703x - 17.86172$  (Figure 6),



**Figure 6.** The representation of the  $INL_{ADC8K}$  to be tested

where  $x$  represents the input signal amplitude,  $y$  is the expected channel number,  $-17.86172$  is the amplitude at the zero channel and  $0.85703$  is the slope of the fit line and the coefficient is  $R_2 = 0.99975$ . An INL test configuration is shown in Figure 5. From the function of  $y$ , replacing the values  $x_i = (21 \div 9519)$  with  $i$  from 1 to 40 and the function  $y = 0.85703x - 17.86172$  will obtain 40 values of  $C_i$ ; then, calculated  $\Delta C_{\max} = (C_r - C_i)_{\max} = 0.00419$ . Using formula  $INL_{ADC8K} = (\Delta C_{\max}/C_{\max}) \times 100\%$  [1], obtained:  $INL_{ADC8K} = \frac{\Delta C_{\max}}{C_{\max}} \cdot 100\% = \frac{47.022}{8121} \cdot 100\% = 0.58\%$  and  $INL_{RSS}$ :  $INL_{ADC8K-Canberra} = 0.159\%$ . The results are shown in Table 2.

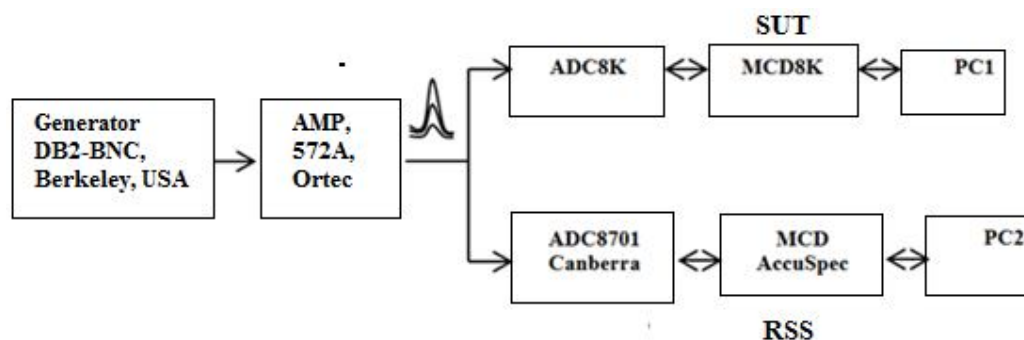
**Table 2.** Integral nonlinearity of system under test and reference standard system

No.	INL%	Value
1	Reference standard system using ADC8K, Canberra	0.159%
2	The system used new ADC8K	0.58%



### 3.2. Differential nonlinearity (DNL) test

To test DNLADC8K, the experiment is arranged as shown in Figure 7. This configuration consists of two independent measuring arms, the upper branch is the ADC containing system that needs to check the technical characteristics formed from the ADC8K, MCD8K, computer, MCANRI data acquisition application program. The lower branch is Canberra's AMP 572A-Ortec, ADC 8701-canberra, MCD Accuspec V1.1, MCA Series 100 application software and computer. DB2 BNC pulse generator-Berkeley gives a positive, unipolar signal to the amplifier input AMP 572A. The shaping time of AMP is chosen as 6  $\mu$ s to reduce the effect of pulse rising time using standard pulse generators. The cycle is as follows:

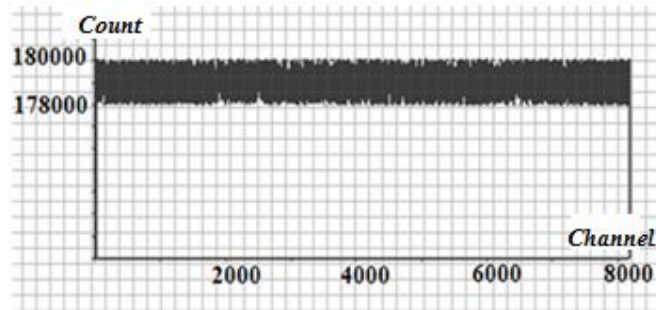


**Figure 7.** Configuration for DNLADC8K differential nonlinearity test

1. Set up the 50 ns rising time and 100  $\mu$ s falling time in the random pulse generator. Calibrate the output signal and select the gain of the AMP 572A so that the unipolar sweep pulse in the MCA following the maximum amplitude range from 1% to 100% (from 0 V to 10 V with 1 second scanning period and preset time of 36000 seconds). The measurement system is set up so that the average count is approximately 36000, reaching a value of 1 pulses per second (cps) from the generator.

2. Start the random pulse generator and data acquisition program in PHA mode. Over time, random data is accumulated in all channels and produces continuous scanning spectra. The differential linearity spectrum of the SUT system is shown in Figure 8. The spectrum consists of 8K pairs of corresponding numbers between the count and the channel and is recorded in the two-dimensional array. For the total count of 8192 channels, the empirical formula is  $\sum_{i=1}^{8192} x_i = 1473706187$ , therefore the mean of counts is:

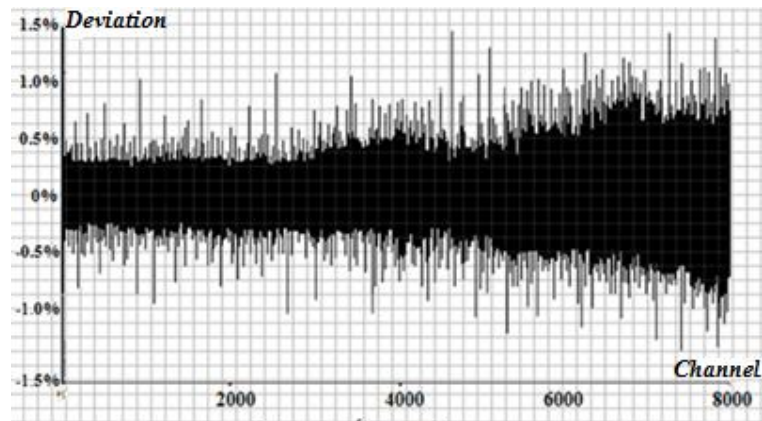




**Figure 8.** Differential linearity spectrum of SUT using ADC8K

$N_{av} = \bar{x} = 179895.7748$ . Apply the formula  $DNL = \frac{\Delta N_{max}}{N_{av}} \cdot 100\%$  [5] and from  $N_{av}$ , find the maximum deviation in 8192 deviation values:

$\Delta N_{max} = (N_x - N_{av})_{max} = 2554.52$ . Thus, the differential nonlinearity of ADC8K is computed as:  $DNL_{ADC8K} = (2554.52/179895.7748) \times 100\% \approx 1.42\%$ . The statistical fluctuation in Figure 9 denotes  $DNL_{ADC8K}$  differential nonlinearity.



**Figure 9.** Differential Nonlinearity of ADC8K

By the same way, the differential nonlinearity of the RSS system is obtained:  $DNL_{RSS} \approx 1.1\%$ ,  $DT_{SUT} = 0.49\%$  and  $DT_{RSS} = 0.41\%$ , respectively. The value pairs of the two systems are shown in Table 3.

**Table 3.**  $SUT_{ADC8K}$  and  $RSS_{Accuspec}$  results of differential nonlinearity tests

No.	Equipment	$T_{meas}$ (s)	$V_{in}$ (mV)	Mode	$t_{AMP}$ ( $\mu$ s)	Range	Counts	DT (%)	DNL (%)
1	$RSS_{Accuspec}$	36000	$10^4$	PHA	6	8192	179128	0.41	1.1
2	$SUT_{ADC8K}$	36000	$10^4$	PHA	6	8192	179012	0.49	1.42

### 3.3. $\chi^2$ test

When dealing with random signals from the radiation source, the quality of the MCA is evaluated by  $\chi^2$ . In the sequence  $n$  the measurement  $x_i$ , the mean  $\bar{x}$  is calculated: Experiment for each measurement is 1000s, conduct 15 continuous measurements and can evaluate the counting quality of the MCA system through  $\chi^2$ . In a series of  $n$  measures  $x_i$ , the mean value is calculated as follows:  $\bar{x} = \frac{\sum_{i=1}^{15} x_i}{n}$ . Experimental variance is calculated by the equation:  $s^2 = \frac{1}{n} \sum_{i=1}^n (x_i - \bar{x})^2$  and  $\chi^2$  is calculated:  $\chi^2 = \frac{(n-1)s^2}{\bar{x}}$ . Experimental values are presented in Tables 4 and 5.

**Table 4.** Synthesis of statistical values to calculate  $\chi^2$

i	$x_i$	$x_i - \bar{x}$	$(x_i - \bar{x})^2$
1	89602	-145.33	21121.8
2	89996	248.67	61835.1
3	89512	-235.33	55381.8
4	89984	236.67	56011.1
5	89979	231.67	53669.4
6	89486	-261.33	68295.1
7	89993	245.67	60352.1
8	89986	238.67	56961.8
9	89481	-266.33	70933.4
10	89632	-115.33	13301.8
11	89977	229.67	52746.8
12	89502	-245.33	60188.4
13	89991	243.67	59373.4
14	89605	-142.33	20258.8
15	89484	-263.33	69344.4
$\bar{x}$	89747.33		
	$\sum_{i=1}^n (x_i - \bar{x})^2$	779775.3	
$s^2$		51985.02	
$\chi^2$		8.109	

**Table 5.** Comparison of  $\chi^2$  results of two SUT and RSS systems

STT	MCA systems	Value
1	$\chi_{SUT}^2$	8.109
2	$\chi_{RSS}^2$	7.495

### 3.4. Check the accuracy of counting and frequency throughput of ADC8K

The accuracy of the count of the ADC8K test system identified by configuration 5 using a DB2-BNC, Berkeley, USA pulse generator is as follows: two SUT and RSS must be set at the same shaping time, maintain all checks and be triggered at the same time for recording and stopping when the preset time ends; pulse generator is started by manual, selectable frequencies are in the range from  $f_{\min} = 90$  Hz to  $f_{\max} = 1$  MHz, preset time  $t_{pr} = 10000$ s; threshold conditions, windows to count are checked for both systems; Performing spectrum measurements in PHA mode, operating in real time mode. The D% deviation between the cumulative counts in the RSS system with the SUT system is called the accuracy of their counts and is calculated by the formula:  $D\% = \frac{C_r - C_t}{C_r} \cdot 100\%$  [5]; where,  $C_r$  is the number of recorded count in the RSS and  $C_t$  is the cumulative count in the SUT. As the elapsed time passes by the preset time  $t_{pr}$ , the measurement system automatically stops. The results of cumulative counts over time and counting differences between the two systems are presented in Table 6.

**Table 6.** Cumulative real-time counts  
and counting differences between two measurement systems

No.	Meas. time	Frequencies	Count $C_r$ in RSS	Count $C_t$ in SUT	Count differences
1	$t_{pr} = 10000$ s	$f_{\min} = 90$ Hz	898836	899437	$D_1 \% = 0.067$
2	$t_{pr} = 10000$ s	$f = 500$ Hz	4978236	4984116	$D_2 \% = 0.118$
3	$t_{pr} = 10000$ s	$f = 1$ kHz	9937265	9942387	$D_3 \% = 0.052$
4	$t_{pr} = 10000$ s	$f_{\max} = 200$ kHz	197946537	198237482	$D_4 \% = 0.147$
5	$t_{pr} = 10000$ s	$f_{\max} = 700$ kHz	6974822513	6989237289	$D_5 \% = 0.207$
6	$t_{pr} = 10000$ s	$f_{\max} = 1$ MHz	9824738239	9857324675	$D_6 \% = 0.332$

### 3.5. Results and comments

When the technical parameters of the instrument are checked, the use of the RSS as a basis for evaluating the operating mode as well as the reliability of the practical method is reflected in the actual data. Experiments presented in the tables. As shown in Table 2, the  $INL_{ADC8K}$  Integral Nonlinearity is higher approximately 3.7 times that of  $INL_{MCD8K-Accuspec}$ , therefore, it affects on the peak stabilization; however, since it does not exceed 1%, it is within acceptable tolerances. In addition,  $R^2 = 0.99975$  shows a strong correlation between the amplitude and the channel corresponding to the statistical fluctuation of 0.025%. Table 3 shows that the differential nonlinearity of the ADC8K block is relatively good as compared to the reference DNL, the deviation is  $|1.1 - 1.42| / 1.1 = 0.291$ . It means it is 1.291 times higher than the standard reference. As such,  $DNL_{ADC8K}$  is not up to standard, but it is acceptable [5]. For 15  $\chi^2$  test measurements, if the results of  $\chi^2$  are in the range of (3.325 ÷ 16.919), those statistics have a normal statistical fluctuation [6] with a 95% confidence interval. Tables 4 and 5 show that  $\chi^2$  of ADC8K satisfies the given condition, so the reliability is high enough for fluctuations in counts. According to the data in Table 6, results of checking the accuracy of counting and input frequency of ADC8K shows that the deviation  $D1\% \div D4\% < 0.15\%$  is relatively good when input pulse does not exceed 200 kHz. Results shows that  $D5\%$  and  $D6\%$  reached 0.332%. Thus, when the input pulse frequency is large enough (from 700kHz or more), the difference in count is relatively higher than normal. This is one of the limitations of newly fabricated ADC8K block that has to be overcome. Therefore, to avoid data loss and to reduce deadtime, the pulse frequency used must be less than 700 kHz.

## 4. Conclusions

Study and application of the 8K ADC block method in a successive approximation using new generation electronics components with variable time and fast acquisition of 2.2  $\mu$ s. This is the most effective method has been focused on research, exploitation to fabricate instrument according to specific objectives: successive approximation ADC, Configuration for channel width uncertainty, D/ A conversion. Based on that, the ADC unit has formed and put into practical application in training. The works presented tests, discussed the experimental results of measuring and checking the parameters and technical specifications of the instrument. Specifically, the technical characteristics of the equipment to be tested; configuration of the reference standard system (RSS) with the system to be evaluated (SUT) for data acquisition and calibration; the results was discussed. It can be said that the new point of academic work is research, successful application of analog signal conversion method of radiation events by successive approximation register (SAR) techniques. To solve this problem, the project incorporates the use of fast-conversion

device (2.2  $\mu$ s/13 bits) with external circuits to offset channel width uncertainty to improve the resolution of the instrument.

The ADC8K block has the following parameters and specifications: Resolution-8192 channels; Variable time 2.2 $\mu$ s; The upper and lower thresholds for the ADC are controlled by software; Input receives positive unipolar signal, amplitude range [0  $\div$  10] V; Integral nonlinearity  $INL_{ADC8K} \approx 0.58\%$  of the full range; Differential nonlinearity  $DNL_{ADC8K} \approx 1.42\%$  for the measuring range;  $\chi^2 = 8.109$ . The application of the newly developed instrument can be used in a multichannel analyzer, Compton suppression spectrometer, or gamma-gamma coincident spectrometer for measuring ionization radiation.

❖ **Conflict of Interest:** Authors have no conflict of interest to declare.

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